4040

SINGLE CHIP 4-BIT
P-CHANNEL MICROPROCESSOR

- Functionally and Electrically
  Upward Compatible to 4004 CPU
- 14 Additional Instructions
  (60 total) Including Logical
  Operations and Read Program
  Memory
- Interrupt Capability
- Single Step Operation
- 8K Byte Memory Addressing
  Capability
- 24 Index Registers
- Subroutine Nesting to 7 Levels
- Standard Operating
  Temperature Range of
  0° to 70°C
- Also Available With -40°
  to +85°C Operating Range

The Intel® 4040 is a complete 4-bit parallel central processing unit (CPU). The CPU can directly address 4K eight bit instruction words or 8K with a bank switch. Seven levels of subroutine nesting, including interrupt, and 24 randomly accessible index registers (24x4) are provided as convenient facilities for the designer. The index registers may be used for addressing or for scratch pad memory for storing computation results. The interrupt feature permits a normal program sequence to be interrupted, with normal program execution continuing after the interrupt service routine is completed. Provisions have also been made to permit single-stepping the CPU using the STOP and ACKNOWLEDGE signals.

The 4040 is an enhanced version of the 4004 and as such retains all the functional capability of that device. It will execute all the 4004 instructions, and is also electrically compatible with all components used with a 4004 CPU.
**Pin Description**

**D<sub>0</sub>-D<sub>3</sub>**
Bidirectional Data Bus. All address and data communication between the processor and the RAM and ROM chips occurs on these 4 lines.

**STP**
STOP input. A logic "1" level on this input causes the processor to enter the STOP mode.

**STPA**
STOP ACKNOWLEDGE output. This signal is present when the processor is in the stopped state. Output is "open drain" requiring pull-down resistor to V<sub>DD</sub>.

**INT**
INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

**INTA**
INTERRUPT ACKNOWLEDGE output. This signal acknowledges receipt of an INTERRUPT signal and prevents additional INTERRUPTS from entering the processor. It remains active until cleared by the execution of the new BRANCH BACK and SRC (BBS) instruction. The output is "open drain" requiring a pull-down resistor to V<sub>DD</sub>.

**RESET**
RESET input. A logic "1" level at this input clears all flag and status registers and forces the program counter to zero. To completely clear all address and index registers, RESET must be applied for 96 clock cycles (12 machine cycles).

**TEST**
TEST input. The logical state of this signal may be tested with the JCN instruction.

**SYNC**
SYNC output. Synchronization signal generated by the processor and sent to ROM and RAM chips. It indicates the beginning of an instruction cycle.

**CM-ROM<sub>0</sub> - CM-ROM<sub>3</sub>**
CM-ROM outputs. These are bank selection signals for the 4002 RAM chips in the system.

**CM-ROM<sub>0</sub> - CM-ROM<sub>1</sub>**
CM-ROM outputs. These are bank selection signals for program ROM chips in the system.

**CY**
CARRY output. The state of the carry flip-flop is present on this output and updated each X<sub>1</sub> time. Output is "open-drain" requiring pull down resistor to V<sub>DD</sub>.

- φ<sub>1</sub>, φ<sub>2</sub> Two phase clock inputs
- V<sub>SS</sub> Most positive voltage
- V<sub>DD</sub> V<sub>SS</sub>−15V ±5% – Main supply voltage
- V<sub>DD1</sub> V<sub>SS</sub>−15V ±5% – Timing supply voltage
- V<sub>DD2</sub> Output buffer supply voltage

*For low power operation
**May vary depending on system interface
Instruction Set Format

A. Machine Instructions

- 1 word instruction - 8 bits requiring 8 clock periods (1 instruction cycle)
- 2 word instruction - 16 bits requiring 16 clock periods (2 instruction cycles)

Each instruction is divided into two 4-bit fields. The upper 4-bits is the OPR field containing the operation code. The lower 4-bits is the OPA field containing the modifier. For two word instructions, the second word contains address information or data.

The upper 4-bits (OPR) will always be fetched before the lower 4-bits (OPA) during M1 and M2 times respectively.

Table I. Machine Instruction Format.

B. Input/Output and RAM Instructions and Accumulator Group Instructions

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed. Table II illustrates the contents of each 4-bit field.

Table II. I/O and Accumulator Group Instruction Formats.
# 4040 Instruction Set

## BASIC INSTRUCTIONS (* = 2 Word Instructions)

<table>
<thead>
<tr>
<th>Hex Code</th>
<th>MMEMONIC</th>
<th>OPR</th>
<th>OPA</th>
<th>DESCRIPTION OF OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>NOP</td>
<td>00 0 0</td>
<td>0 0 0 0</td>
<td>No operation</td>
</tr>
<tr>
<td>01</td>
<td>*JON</td>
<td>00 0 0 0 1</td>
<td>C C C C A A A A A A</td>
<td>Jump to ROM address A A A A A A A A A A (within the same ROM that contains this JON instruction) if condition C C C C is true, otherwise go to the next instruction in sequence</td>
</tr>
<tr>
<td>02</td>
<td>*FIN</td>
<td>00 0 1 0 0 0 1 1 1</td>
<td>R R R R 0 0 0 0</td>
<td>Fetch immediate (direct) from ROM Data D D D D D D D D</td>
</tr>
<tr>
<td>03</td>
<td>JIN</td>
<td>00 0 1 1 1 1</td>
<td>R R R R</td>
<td>Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR</td>
</tr>
<tr>
<td>04</td>
<td>JUN</td>
<td>00 1 0 0 0 0 0 0 0 0</td>
<td>A A A A A A A A A A</td>
<td>Jump unconditional to ROM address A A A A A A A A A A</td>
</tr>
<tr>
<td>05</td>
<td>*JMS</td>
<td>00 1 0 1 1 1</td>
<td>A A A A A A A 0</td>
<td>Jump to subroutine ROM address A A A A A A A A A A</td>
</tr>
<tr>
<td>06</td>
<td>INC</td>
<td>01 1 1 1 1 1</td>
<td>R R R R 0 0 0 0</td>
<td>Increment contents of register RRRR</td>
</tr>
<tr>
<td>07</td>
<td>*ISZ</td>
<td>01 1 1 1 1 1</td>
<td>R R R R A A A A A 0</td>
<td>Increment contents of register RRRR. Go to ROM address A A A A A A A (within the same ROM that contains this ISZ instruction) if result = 0, otherwise go to the next instruction in sequence</td>
</tr>
<tr>
<td>08</td>
<td>ADD</td>
<td>01 0 0 0 0 0 0 0 0</td>
<td>R R R R</td>
<td>Add contents of register RRRR to accumulator with carry</td>
</tr>
<tr>
<td>09</td>
<td>SUB</td>
<td>01 0 0 1 1 1 1</td>
<td>R R R R</td>
<td>Subtract contents of register RRRR to accumulator with borrow</td>
</tr>
<tr>
<td>10</td>
<td>LO</td>
<td>01 0 1 0 0 0 0 0 0 0</td>
<td>R R R R</td>
<td>Load contents of register RRRR to accumulator</td>
</tr>
<tr>
<td>11</td>
<td>XCH</td>
<td>01 0 1 1 1 1</td>
<td>R R R R</td>
<td>Exchange contents of index register RRRR and accumulator</td>
</tr>
<tr>
<td>12</td>
<td>BBL</td>
<td>11 0 0 0 0 0 0 0 0</td>
<td>D D D D</td>
<td>Branch back (down 1 level in stack) and load data DDDD to accumulator</td>
</tr>
<tr>
<td>13</td>
<td>LDM</td>
<td>11 0 1 1 1 1 1 1 1 1 1</td>
<td>D D D D</td>
<td>Load data DDDD to accumulator</td>
</tr>
<tr>
<td>14</td>
<td>CLB</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Clear both. (Accumulator and carry)</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>DLC</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Clear carry</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>IAC</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Increment accumulator</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>CMC</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Complement carry</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>CMA</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Complement accumulator</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>RAL</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Rotate left. (Accumulator and carry)</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>RAR</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Rotate right. (Accumulator and carry)</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>TCC</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Transmit carry to accumulator and clear carry</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>DAC</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Decrement accumulator</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>TCS</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Transfer carry subtract and clear carry</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>STC</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Set carry</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>DAA</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Decimal adjust accumulator</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>KBP</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>DCL</td>
<td>11 1 1 1 1 1 1 1 1 1 1</td>
<td>Designate command line</td>
<td></td>
</tr>
</tbody>
</table>

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5-14
### 4040 ONLY INSTRUCTIONS

<table>
<thead>
<tr>
<th>Hex Code</th>
<th>MNEMONIC</th>
<th>D1, D2, D3, D4</th>
<th>OPA</th>
<th>D1, D2, D3, D4</th>
<th>DESCRIPTION OF OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>HLT</td>
<td>0 0 0 0 0 0 0 1</td>
<td></td>
<td></td>
<td>Executes Halt until interrupt received.</td>
</tr>
<tr>
<td>02</td>
<td>BBS</td>
<td>0 0 0 0 0 0 1 0</td>
<td></td>
<td></td>
<td>Return from subroutine and restore SRC.</td>
</tr>
<tr>
<td>03</td>
<td>LCR</td>
<td>0 0 0 0 0 0 1 1</td>
<td></td>
<td></td>
<td>Data RAM and ROM bank status loaded into ACC.</td>
</tr>
<tr>
<td>04</td>
<td>OR4</td>
<td>0 0 0 0 0 0 1 0</td>
<td></td>
<td></td>
<td>OR accumulator with IR4.</td>
</tr>
<tr>
<td>05</td>
<td>OR5</td>
<td>0 0 0 0 0 1 0 1</td>
<td></td>
<td></td>
<td>OR accumulator with IR5.</td>
</tr>
<tr>
<td>06</td>
<td>AN4</td>
<td>0 0 0 0 0 1 1 0</td>
<td></td>
<td></td>
<td>AND accumulator with IR4.</td>
</tr>
<tr>
<td>07</td>
<td>AN5</td>
<td>0 0 0 0 0 1 1 1</td>
<td></td>
<td></td>
<td>AND accumulator with IR5.</td>
</tr>
<tr>
<td>08</td>
<td>UBO</td>
<td>0 0 0 0 1 0 0 0</td>
<td></td>
<td></td>
<td>Select ROM bank 0.</td>
</tr>
<tr>
<td>09</td>
<td>SBI</td>
<td>0 0 0 0 1 0 0 1</td>
<td></td>
<td></td>
<td>Select ROM bank 1.</td>
</tr>
<tr>
<td>0A</td>
<td>SBO</td>
<td>0 0 0 0 1 0 1 0</td>
<td></td>
<td></td>
<td>Select IR bank 0.</td>
</tr>
<tr>
<td>0B</td>
<td>SBI</td>
<td>0 0 0 0 1 1 0 1</td>
<td></td>
<td></td>
<td>Select IR bank 1.</td>
</tr>
<tr>
<td>0C</td>
<td>EIN</td>
<td>0 0 0 0 1 1 0 0</td>
<td></td>
<td></td>
<td>Enable interrupt detection.</td>
</tr>
<tr>
<td>0D</td>
<td>DIN</td>
<td>0 0 0 0 1 1 0 1</td>
<td></td>
<td></td>
<td>Disable interrupt detection.</td>
</tr>
<tr>
<td>0E</td>
<td>RPM</td>
<td>0 0 0 0 1 1 1 0</td>
<td></td>
<td></td>
<td>Load accumulator from 4269-controlled program RAM.</td>
</tr>
</tbody>
</table>

### 4001/4002/4008/4009/4289 INPUT/OUTPUT AND RAM INSTRUCTIONS

<table>
<thead>
<tr>
<th>Hex Code</th>
<th>MNEMONIC</th>
<th>D1, D2, D3, D4</th>
<th>OPA</th>
<th>D1, D2, D3, D4</th>
<th>DESCRIPTION OF OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>SRC</td>
<td>0 0 1 0 R R R 1</td>
<td></td>
<td></td>
<td>Send register control. Send the address (contents of index register pair RR) to ROM and RAM at XH and XL time in the instruction cycle.</td>
</tr>
<tr>
<td>0E</td>
<td>WRM</td>
<td>1 1 1 0 0 0 0 0</td>
<td></td>
<td></td>
<td>Write the contents of the accumulator into the previously selected RAM main memory character.</td>
</tr>
<tr>
<td>0E</td>
<td>WMP</td>
<td>1 1 1 0 0 0 1 0</td>
<td></td>
<td></td>
<td>Write the contents of the accumulator into the previously selected RAM output port. (Output Lines)</td>
</tr>
<tr>
<td>0E</td>
<td>WRR</td>
<td>1 1 1 0 0 0 0 1</td>
<td></td>
<td></td>
<td>Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)</td>
</tr>
<tr>
<td>0E</td>
<td>WPM</td>
<td>1 1 1 0 0 1 1 0</td>
<td></td>
<td></td>
<td>Write the contents of the accumulator into the previously selected half byte of read/write program memory (used with 4008/4009 or 4289 only)</td>
</tr>
<tr>
<td>0E</td>
<td>WR0</td>
<td>1 1 1 0 0 1 0 0</td>
<td></td>
<td></td>
<td>Write the contents of the accumulator into the previously selected RAM status character 0.</td>
</tr>
<tr>
<td>0E</td>
<td>WR1</td>
<td>1 1 1 0 0 1 0 1</td>
<td></td>
<td></td>
<td>Write the contents of the accumulator into the previously selected RAM status character 1.</td>
</tr>
<tr>
<td>0E</td>
<td>WR2</td>
<td>1 1 1 0 0 1 1 0</td>
<td></td>
<td></td>
<td>Write the contents of the accumulator into the previously selected RAM status character 2.</td>
</tr>
<tr>
<td>0E</td>
<td>WR3</td>
<td>1 1 1 0 1 0 1 1</td>
<td></td>
<td></td>
<td>Write the contents of the accumulator into the previously selected RAM status character 3.</td>
</tr>
<tr>
<td>0E</td>
<td>SBM</td>
<td>1 1 1 0 1 0 0 0</td>
<td></td>
<td></td>
<td>Subtract the previously selected RAM main memory character from accumulator with borrow.</td>
</tr>
<tr>
<td>0E</td>
<td>RDM</td>
<td>1 1 1 0 1 0 0 1</td>
<td></td>
<td></td>
<td>Read the previously selected RAM main memory character into the accumulator.</td>
</tr>
<tr>
<td>0E</td>
<td>RDR</td>
<td>1 1 1 0 1 0 1 0</td>
<td></td>
<td></td>
<td>Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)</td>
</tr>
<tr>
<td>0E</td>
<td>AMD</td>
<td>1 1 1 0 1 0 1 1</td>
<td></td>
<td></td>
<td>Add the previously selected RAM main memory character to accumulator with carry.</td>
</tr>
<tr>
<td>0E</td>
<td>RD0</td>
<td>1 1 1 0 1 1 0 0</td>
<td></td>
<td></td>
<td>Read the previously selected RAM status character 0 into accumulator.</td>
</tr>
<tr>
<td>0E</td>
<td>RD1</td>
<td>1 1 1 0 1 1 0 1</td>
<td></td>
<td></td>
<td>Read the previously selected RAM status character 1 into accumulator.</td>
</tr>
<tr>
<td>0E</td>
<td>RD2</td>
<td>1 1 1 0 1 1 1 0</td>
<td></td>
<td></td>
<td>Read the previously selected RAM status character 2 into accumulator.</td>
</tr>
<tr>
<td>0E</td>
<td>RD3</td>
<td>1 1 1 0 1 1 1 1</td>
<td></td>
<td></td>
<td>Read the previously selected RAM status character 3 into accumulator.</td>
</tr>
<tr>
<td>Hex Mnemonic</td>
<td>Hex Mnemonic</td>
<td>Hex Mnemonic</td>
<td>Hex Mnemonic</td>
<td></td>
<td></td>
</tr>
<tr>
<td>--------------</td>
<td>--------------</td>
<td>--------------</td>
<td>--------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 NOP</td>
<td>40 JUN</td>
<td>80 ADD 0</td>
<td>C0 BBL 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01 HLT</td>
<td>41 JUN</td>
<td>81 ADD 1</td>
<td>C1 BBL 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>02 BBS</td>
<td>42 JUN</td>
<td>82 ADD 2</td>
<td>C2 BBL 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>03 LDR</td>
<td>43 JUN</td>
<td>83 ADD 3</td>
<td>C3 BBL 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>04 OR4</td>
<td>44 JUN</td>
<td>84 ADD 4</td>
<td>C4 BBL 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>05 OR5</td>
<td>45 JUN</td>
<td>85 ADD 5</td>
<td>C5 BBL 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>06 AN6</td>
<td>46 JUN</td>
<td>86 ADD 6</td>
<td>C6 BBL 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>07 AN7</td>
<td>47 JUN</td>
<td>87 ADD 7</td>
<td>C7 BBL 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>08 DBO</td>
<td>48 JUN</td>
<td>88 ADD 8</td>
<td>C8 BBL 8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>09 DB1</td>
<td>49 JUN</td>
<td>89 ADD 9</td>
<td>C9 BBL 9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0A SB0</td>
<td>4A JUN</td>
<td>8A ADD 10</td>
<td>CA BBL 10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0B SB1</td>
<td>4B JUN</td>
<td>88 ADD 11</td>
<td>CB BBL 11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0C EIN</td>
<td>4C JUN</td>
<td>8C ADD 12</td>
<td>CD BBL 12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0D DFN</td>
<td>4D JUN</td>
<td>8D ADD 13</td>
<td>CD BBL 13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0E RPM</td>
<td>4E JUN</td>
<td>8E ADD 14</td>
<td>CE BBL 14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F –</td>
<td>4F JUN</td>
<td>8F ADD 15</td>
<td>CF BBL 15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 JCN CN=0</td>
<td>50 JMS</td>
<td>90 SUB 0</td>
<td>DD LDM 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 JCN CN=1 also JNT</td>
<td>51 JMS</td>
<td>91 SUB 1</td>
<td>DD LDM 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12 JCN CN=2 also JC</td>
<td>52 JMS</td>
<td>92 SUB 2</td>
<td>DD LDM 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13 JCN CN=3</td>
<td>53 JMS</td>
<td>93 SUB 3</td>
<td>DD LDM 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14 JCN CN=4 also JZ</td>
<td>54 JMS</td>
<td>94 SUB 4</td>
<td>DD LDM 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15 JCN CN=5</td>
<td>55 JMS</td>
<td>95 SUB 5</td>
<td>DD LDM 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 JCN CN=6</td>
<td>56 JMS</td>
<td>96 SUB 6</td>
<td>DD LDM 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17 JCN CN=7</td>
<td>57 JMS</td>
<td>97 SUB 7</td>
<td>DD LDM 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18 JCN CN=8</td>
<td>58 JMS</td>
<td>98 SUB 8</td>
<td>DD LDM 8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19 JCN CN=9 also JT</td>
<td>59 JMS</td>
<td>99 SUB 9</td>
<td>DD LDM 9</td>
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<td>5A JMS</td>
<td>9A SUB 10</td>
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<td>1B JCN CN=11</td>
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<td>DD LDM 11</td>
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<td>1C JCN CN=12 also JNZ</td>
<td>5C JMS</td>
<td>9C SUB 12</td>
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<td>E0 WRM</td>
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<td>AB LD 11</td>
<td>EA RD2</td>
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<td>EC RD0</td>
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<td>30 FIN 0</td>
<td>70 ISZ 0</td>
<td>80 XCH 0</td>
<td>F0 CLB</td>
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<td>31 JIN 0</td>
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<td>72 ISZ 2</td>
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<td>75 ISZ 5</td>
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<td>76 ISZ 6</td>
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<td>77 ISZ 7</td>
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<td>F7 TCC</td>
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<td>39 JIN 8</td>
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<td>7A ISZ 10</td>
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<td>FA STC</td>
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<td>3B JIN 10</td>
<td>7B ISZ 11</td>
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<td>FC KBP</td>
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<td>7E ISZ 14</td>
<td>94 XCH 14</td>
<td>FE –</td>
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<td>3F JIN 14</td>
<td>7F ISZ 15</td>
<td>95 XCH 15</td>
<td>FF –</td>
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# Absolute Maximum Ratings*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Limit</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{SB}</td>
<td>Standby Supply Current (V_{DD1} + V_{DD2})</td>
<td>3</td>
<td>5</td>
<td></td>
<td>mA</td>
<td>T_{A} = 25°C, V_{DD} = V_{SS}</td>
</tr>
<tr>
<td>I_{DD} (total)</td>
<td>Supply Current (V_{DD} + V_{DD1} + V_{DD2})</td>
<td>40</td>
<td>60</td>
<td></td>
<td>mA</td>
<td>T_{A} = 25°C</td>
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## D.C. and Operating Characteristics

T_{A} = 0°C to 70°C; V_{SS} = V_{DD} = 15V ±5%; t_{PW} = t_{D1} = 400 nsec; t_{D2} = 150 nsec; 4040 V_{DD1} = V_{DD2} = V_{DD}; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise specified.

### SUPPLY CURRENT

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Input Leakage Current</th>
<th>10</th>
<th>µA</th>
<th>V_{IL} = V_{DD}</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IH}</td>
<td>Input High Voltage (Except Clocks)</td>
<td>V_{SS} -1.5</td>
<td>V_{SS} +3</td>
<td>V</td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Input Low Voltage (Except Clocks)</td>
<td>V_{DD}</td>
<td>V_{SS} -5.5</td>
<td>V</td>
</tr>
<tr>
<td>V_{LO}</td>
<td>Input Low Voltage</td>
<td>V_{DD}</td>
<td>V_{SS} -4.2</td>
<td>V</td>
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<tr>
<td>V_{HC}</td>
<td>Input High Voltage Clocks</td>
<td>V_{SS} -1.5</td>
<td>V_{SS} +3</td>
<td>V</td>
</tr>
<tr>
<td>V_{LC}</td>
<td>Input Low Voltage Clocks</td>
<td>V_{DD}</td>
<td>V_{SS} -13.4</td>
<td>V</td>
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### INPUT CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Data Bus Output Leakage Current</th>
<th>10</th>
<th>µA</th>
<th>V_{OUT} ~12V</th>
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</thead>
<tbody>
<tr>
<td>V_{OH}</td>
<td>Output High Voltage</td>
<td>V_{SS} -5V</td>
<td>V_{SS}</td>
<td>V</td>
</tr>
<tr>
<td>I_{DL}</td>
<td>Data Lines Sinking Current</td>
<td>8</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td>V_{IL}</td>
<td>CM-ROM Sinking Current</td>
<td>6.5</td>
<td>12</td>
<td>mA</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>CM-ROM Sinking Current</td>
<td>2.5</td>
<td>6</td>
<td>mA</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Output Low Voltage, Data Bus, CM, SYNC</td>
<td>V_{SS} -12</td>
<td>V_{SS} -6.5</td>
<td>V</td>
</tr>
<tr>
<td>R_{OH}</td>
<td>Output Resistance, Data Line &quot;0&quot; Level</td>
<td>150</td>
<td>250</td>
<td>Ω</td>
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<tr>
<td>R_{OH}</td>
<td>CM-ROM Output Resistance, Data Line &quot;0&quot; Level</td>
<td>320</td>
<td>600</td>
<td>Ω</td>
</tr>
<tr>
<td>R_{OH}</td>
<td>CM-ROM Output Resistance, Data Line &quot;0&quot; Level</td>
<td>250</td>
<td>500</td>
<td>Ω</td>
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<tr>
<td>R_{OH}</td>
<td>INTA, CY, STPA Output Resistance &quot;0&quot; Level</td>
<td>1.1</td>
<td>1.8</td>
<td>kΩ</td>
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### Capacitance

<table>
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<tr>
<th>Symbol</th>
<th>Clock Capacitance</th>
<th>17</th>
<th>25</th>
<th>pF</th>
<th>V_{IN} = V_{SS}</th>
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<tr>
<td>C_{DB}</td>
<td>Data Bus Capacitance</td>
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<td>10</td>
<td>pF</td>
<td>V_{IN} = V_{SS}</td>
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<tr>
<td>C_{IN}</td>
<td>Input Capacitance</td>
<td>10</td>
<td>pF</td>
<td>V_{IN} = V_{SS}</td>
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</tr>
<tr>
<td>C_{OUT}</td>
<td>Output Capacitance</td>
<td>10</td>
<td>pF</td>
<td>V_{IN} = V_{SS}</td>
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### Typical D.C. Characteristics

![Graph showing 4040 IDD vs. Temperature]

### A.C. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limit</th>
<th>Unit</th>
<th>Conditions</th>
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</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;CY&lt;/sub&gt;</td>
<td>Clock Period</td>
<td>1.35 - 2.0</td>
<td>μsec</td>
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<tr>
<td>t&lt;sub&gt;R1&lt;/sub&gt;</td>
<td>Clock Rise Time</td>
<td>50 ns</td>
<td></td>
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<tr>
<td>t&lt;sub&gt;F&lt;/sub&gt;</td>
<td>Clock Fall Times</td>
<td>50 ns</td>
<td></td>
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<tr>
<td>t&lt;sub&gt;W&lt;/sub&gt;</td>
<td>Clock Width</td>
<td>380 - 480 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;D1&lt;/sub&gt;</td>
<td>Clock Delay φ&lt;sub&gt;1&lt;/sub&gt; to φ&lt;sub&gt;2&lt;/sub&gt;</td>
<td>400 - 650 ns</td>
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<tr>
<td>t&lt;sub&gt;D2&lt;/sub&gt;</td>
<td>Clock Delay φ&lt;sub&gt;2&lt;/sub&gt; to φ&lt;sub&gt;1&lt;/sub&gt;</td>
<td>150 ns</td>
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<tr>
<td>t&lt;sub&gt;N&lt;/sub&gt;</td>
<td>Data-In, CM, SYNC, Write Time</td>
<td>350 - 100 ns</td>
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<tr>
<td>t&lt;sub&gt;WRPM&lt;/sub&gt;</td>
<td>Data-In Hold Time-RPM Instruction (X&lt;sub&gt;2&lt;/sub&gt; state)</td>
<td>350 - 100 ns</td>
<td></td>
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</tr>
<tr>
<td>t&lt;sub&gt;W1(1,3)&lt;/sub&gt;</td>
<td>Data-In, CM, SYNC Hold Time</td>
<td>40 - 20 ns</td>
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<tr>
<td>t&lt;sub&gt;WRPM&lt;/sub&gt;</td>
<td>Data-In Write Time-RPM Instruction (X&lt;sub&gt;2&lt;/sub&gt; state)</td>
<td>40 - 20 ns</td>
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<tr>
<td>t&lt;sub&gt;W3(3)&lt;/sub&gt;</td>
<td>Data Bus Hold Time During</td>
<td>150 ns</td>
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<tr>
<td>t&lt;sub&gt;SH&lt;/sub&gt;(2)</td>
<td>Set Time (Reference)</td>
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<tr>
<td>t&lt;sub&gt;DACO&lt;/sub&gt;(5)</td>
<td>Data-Out Access Time</td>
<td>930 ns</td>
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<td></td>
<td>Data Lines</td>
<td>930 ns</td>
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<td></td>
<td>Sync</td>
<td>700 ns</td>
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<td></td>
<td>CM-ROM</td>
<td>930 ns</td>
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<tr>
<td></td>
<td>CM-RAM</td>
<td>930 ns</td>
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<td>t&lt;sub&gt;DH&lt;/sub&gt;</td>
<td>Data-Out Hold Time</td>
<td>50 - 150 ns</td>
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<tr>
<td>t&lt;sub&gt;DEL&lt;/sub&gt;</td>
<td>CY, STPACK, INTACK Delay</td>
<td>2.0 μsec</td>
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</table>

### NOTES:
1. t<sub>D</sub> measured with t<sub>CS</sub> = 10 ns.
2. t<sub>DACO</sub> is Data Bus, Sync and CM-line output access time referred to the φ<sub>2</sub> trailing edge which clocks these lines out.
3. t<sub>CS</sub> is the same output access time referred to the leading edge of the next φ<sub>2</sub> clock pulse.
4. All components which may transmit instruction or data to the 4040 at X<sub>2</sub> always enter a float state until the 4040 takes over the data bus at X<sub>3</sub> time. Therefore the t<sub>DH</sub> requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1μV/μs.
5. The 4040 accumulator is gated out at X<sub>1</sub> time at φ<sub>1</sub> leading edge, and the t<sub>DACO</sub> is 930 nsec + t<sub>SH2</sub>.
Figure 1. Timing Diagram.

Figure 2. Timing Detail.
Figure 3. Stop Timing.

Figure 4. Halt Timing (Exit Using Stop Input).

Figure 5. Interrupt Timing.
Figure 6. Halt Timing (Exit Using Interrupt).